GCC1702B "MARIA" CHIP

Acceptance Specification
(Atari Part #C024674-30 Drawing)

March 21, 1984

GENERAL COMPUTER COMPANY

CONFIDENTIAL

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1.0 Scope

This document is intended to be the acceptance specification to the GCC1702B "Maria" video graphics controller chip designed by General Computer Company. It describes all important functional, timing, and parametric information peculiar to this device.

2.1 Features

The chip is a graphics controller for interfacing NTSC display to a microprocessor (6502) video game system. It replaces the functions of the conventional television interface adapter "TIA" when enabled by a new cartridge, and allows a conventional TIA chip to function normally when a 2600 VCS cartridge is used. The following functions are supported:

* Clock logic which runs the microprocessor at 1.79 MHz when Maria is enabled, and 1.19 MHz when TIA is enabled. An off-chip 14.3 MHz crystal oscillator provides the master system timing signals. This signal is immediately divided by two to provide the internal clock at a 50% duty cycle.

* Chip select logic for controlling two 2k static RAM chips (150 nsec maximum access), a 6532 chip, and the TIA chip.

* Horizontal and vertical timing logic which generates BLANK, SYNC, and color burst signals without processor intervention. In addition, a WSYNC operation allows the processor to sync to the next scanline by negating the READY line.

* A 25 X 8-bit memory for writing color data (four bits of chrominance and four bits of luminance). This memory is write-only to the microprocessor, but may be read by a tester. It may be written during on-screen time with no dramatic color glitches, although a given pixel may be extended as a result.

* Color and luminance circuits, with tri-state luminence outputs to facilitate external selection of Maria or TIA outputs, depending on which chip is enabled.

* Video generation circuitry consisting of two 160 X 5-bit "line ram" buffers. These function as a double-buffered image of a horizontal scan line. During each scanline, one buffer is loaded by the dma controller and the other is synchronously read out through the color and luminence circuits. The line ram has the following features:

  1. Two or four of the 5-bit pixel cells may be written in one operation, on any pixel boundary within the memory.

  2. There is a transparency function applied to writing any pixel, such that if the least significant 2 bits of the data to be written are 00, that pixel is not written. This feature may be disabled by a control register bit (KM).

  3. There is a Burst Clear function for the line ram, which can clear either of the two line buffers to zeroes in one operation.

4. The output steering logic for the line ram allows a given 5-bit call to be interpreted in any of three major ways:

   1. 160-mode: one cell, one pixel on the screen.

   2. 320xi mode: one call, two pixels on the screen, half width. The least significant two bits are used alternately.

   3. 320x2 mode: one cell, two pixels, half-width. The least significant four bits are steered alternately to be the least significent 2 bits of the color ram address, with 0's padded.

   There are variations on these modes allowing combinations of 320xi and 320x2 resolutions on a single scanline at once.

* DMA (Direct Memory Access) circuitry which, once started, halts the microprocessor and loads object information into the line ram at programmable horizontal positions.

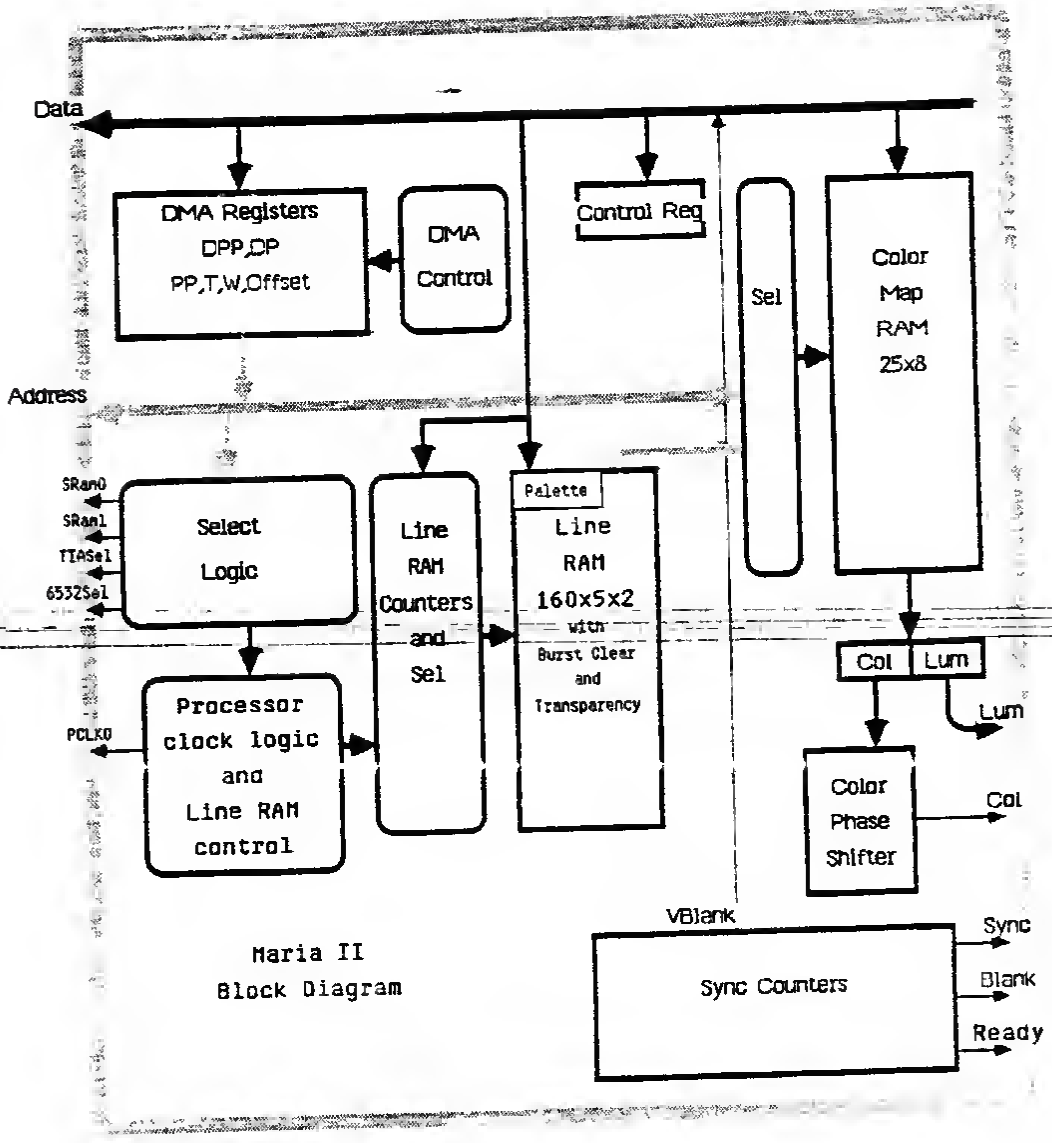
   1. Loading is controlled by a display list of variable sized objects previously set up by the microprocessor program.

   2. Display lists are controlled by Display List Lists, which can also set certain modes of the chip on a vertical basis and provide Display List Interrupts to the microprocessor.

   3. An indirect "character map" mode, which uses a character base byte concatenated with bytes read from a map to form an address for finding graphics.

   4. A "holey DMA" mode, which infers zero graphics data from the effective graphics address generated for an object, saving memory (by not requiring vertical padding of images) and time (by terminating the object's DMA early).

* A Mode ENable line, which controls the memory map generated by the chip select logic to be either the loose map of an Atari 2600 system, or a larger memory system. In addition, the MEN line resets the sync counters to zero when negated.



Maria II
Block Diagram

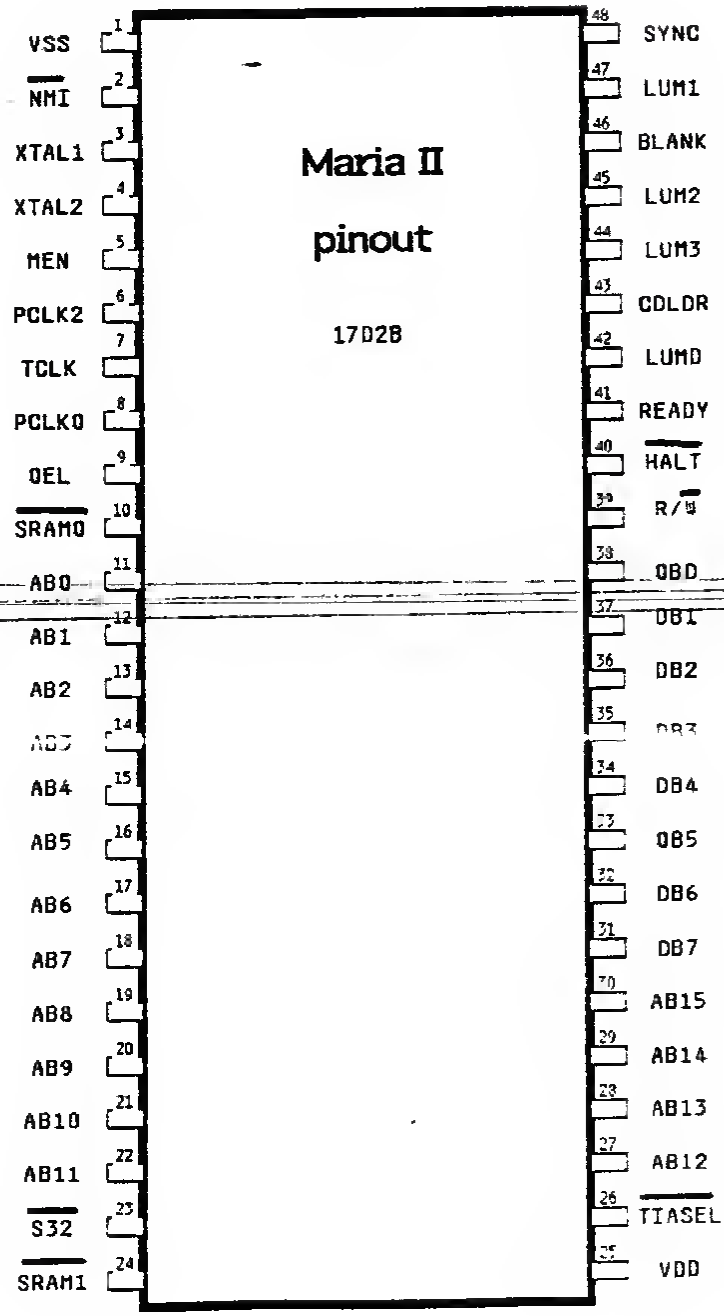
2.2 I/O signals

Maria pin description

Name	pin #	type	function
VSS	1	PWR	Ground
INT-	2	O	Interrupt request output, intended for 6502 NMI-Slow. One MOS load.
XTALI	3	I	Oscillator input 14.318080 MHz nominal
XTALO	4	O	Oscillator output
MEN	5	I	Maria Enable input. When high, maria operates normally When low, video is shut off, chip is held in reset, and memory map is set for 2600-mode. 3-6K pulldown R.
PCLK2	6	I	6502 Phase 2 clock input. Used to synchronize with processor. Not all processor synchronization is done from this pin.
TCLK	7	O	TIA 3.58 MHz clock. Oscillator freq divide by 4. One MOS load.
PCLK0	8	O	6502 Phase 0 clock output. Drives processor at 1.19 or 1.79 MHz. One MOS load.
DEL	9	I*	Delay line control voltage input. Low resistance input
RAM0-	10	O	RAM chip select output. One MOS load.
AB0 thru AB11	11 thru 22	I/O	Address input (when 6502 is in control) or output (during DMA). 150 pF, 2 lsttl loads.
SEL32-	23	O	6532 chip select output. One MOS load.
RAM1-	24	O	RAM chip select output. One MOS load
VDD	25	PWR	+5V
TIA-	26	O	TIA chip select output. One MOS load
AB12 thru AB15	27 thru 30	I/O	Address input (when 6502 is in control) or output (during DMA). 150 pF, 2 lsttl loads
D87 thru D80	31 thru 38	I/O	Data input or output.
R/W-	39	I*	processor r/w- control input. 3-6K pullup resistor on pad to eliminate discretes on pc bd.

HALT-	40	O	Processor halt output. One MOS load.
RDY	41	O*	Ready output to 6502. Open Drain with pullup resistor. One MOS load.
LUM0	42	O*	Least significant video luminance output bit. Pad goes tri-state when Maria not enabled.
COL	43	O*	Color output pin. Pad goes tri-state when Maria not enabled.
LUM3	44	O*	Video luminance outut pin. Pad goes low when Maria not enabled.
LUM2	45	O*	Video luminance outut pin. Pad goes low when Maria not enabled.
BLANK	46	O*	Video blanking output pin. Pad goes tri-state when Maria not enabled.
LUM1	47	O*	Video luminance outut pin. Pad goes low when Maria not enabled.
SYNC	48	O*	Video Sync output pin. Pad goes low when Maria not enabled.

* indicates that pad is unusual; see function description.


Maria II
pinout
17D2B
1 VSS
2 NMI
3 XTAL1
4 XTAL2
5 MEN
6 PCLK2
7 TCLK
8 PCLK0
9 OEL
10 SRAM0
11 AB0
12 AB1
13 AB2
14 AB3
15 AB4
16 AB5
17 AB6
18 AB7
19 AB8
20 AB9
21 AB10
22 AB11
23 S32
24 SRAM1
48 SYNC
47 LUM1
46 BLANK
45 LUM2
44 LUM3
43 CDLDR
42 LUM0
41 READY
40 HALT
39 R/W
38 DB0
37 DB1
36 DB2
35 DB3
34 DB4
33 DB5
32 DB6
31 DB7
30 AB15
29 AB14
28 AB13
27 AB12
26 TIASEL
25 VDD

3.1 Microprocessor Operation

Microprocessor operations are used to set up the control register and pixel color values, which are used in subsequent DMA operations. In addition, a microprocessor read operation is used to detect vertical blank for frame synchronization.

The format of the control register (address $3C) is as follows.

bit7	6	5	4	3	2	1	bit0
CK	DM1	DM0	CWIDTH	BCNTL	KM	RM1	RM0

CK : Color Kill; shuts off color burst to prevent artifacting in 320 text modes.
DMn : DMA mode, see table.
CWIDTH : Char Map width. 1 indicates 2 bytes of graphics per map byte, 0 indicates 1 byte of graphics for each map byte.
BCNTL : Border Control. 1 indicates that the background color will extend into horizontal overscan. 0 indicates overscan will be black.
KM : Kangaroo Mode. 1 disables transparency. Used for some 320 modes.
RMn : Line Ram read mode, see graphics mode table.

DM1	DM0	Meaning
0	0	Test 'eovb'. Do not use.
0	1	Test 'startscan'. Do not use.
1	0	Run normally.
1	1	Inactive.

Setting the DMn bits to the Test modes will cause one entry into the DMA loop, followed by an Inactive state. This mode may not be used by a programmer, however, as this unusual entry into DMA does not assert the HALT pin to the 6502; it simply starts taking over the address bus without asking, causing bus contention.

3.2 Microprocessor Operation (continued)

Following is the 3600-mode register map, specifying the addresses which the Maria chip supports for accessing the color RAM and other registers. The color RAM registers are write-only to the 6502, although a semiconductor test program may read them. The only processor-readable bit in the system is the VBLANK bit of the status register.

Maria-mode Register Map

tw 6/16

Hex Adr	Register	notes.
20	P0C0	Background.
21	P0C1	
22	P0C2	
23	P0C3	
24	WSYNC	write to Strobe for WaitForSync.
25	P1C1	
26	P1C2	
27	P1C3	
28	STATRD	READ: VB 0 0 0 0 0 0
29	P2C1	
2A	P2C2	
2B	P2C3	
2C	DPPH	Write Only
2D	P3C1	
2E	P3C2	
2F	P3C3	
30	DPPL	Displaylist Pointer Pointer Low.
31	P4C1	
32	P4C2	
33	P4C3	
34	CharBase	Write Only
35	P5C1	
36	P5C2	
37	P5C3	
38	Unused	write in 0 (Reserved for future enhancements)
39	P6C1	
3A	P6C2	
3B	P6C3	
3C	CTRL	WRITE: CK DM1 DM0 CWIDTH BCNTL KM RM1 RM0
3D	P7C1	
3E	P7C2	
3F	P7C3	

Maria II Memory Map

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	MEN	PAV	HLT	OUTPUT	
0	0	0	0	0	1	0		1			1			SEL32F	480-4FF, 580-5FF
0	0	0	0	0	0	1		1			1			SEL32F	280-2FF, 380-3FF
			0					1			0			SEL32F	90 - FF
0	0	0	1	1							1		1	SELRAM1F	1800-1FFF
0	0	0	1	1							1	1	0	SELRAM1F	1800-1FFF
			0					0			0			TIASELF	0 - 7F
0	0	0	0	0	0			0	0	0	1			TIASELF	0 - 1F, 100-11F, 200-21F, 300-31F
0	0	0	0	0	0			0	0	1	1	*		PAR23	20 - 3F
0	0	0	0	0	0			1			1		1	SELRAM0F	80 - FF
0	0	0	0	0	0			1			1	1	0	SELRAM0F	80 - FF
0	0	0	0	0	0			0	1		1		1	SELRAM0F	40 - 7F
0	0	0	0	0	0			0	1		1	1	0	SELRAM0F	40 - 7F, 040-0FF, 140-1FF, 240-2FF, 340-3FF
0	0	1	0	0							1		1	SELRAM0F	2000-27FF
0	0	1	0	0							1	1	0	SELRAM0F	2000-27FF
											0			SLOW	
0	0	0	0	0	0			0	0	0	1			SLOW	(TIA)
0	0	0	0	0	1	0		1			1			SLOW	(6532)
0	0	0	0	0	0	1		1			1			SLOW	(6532)

1. Blank address bits are don't cares.

2. PAV is "Processor Address Valid," an internal signal which is PCLK0 OR PCLK2.

3. The SLOW outputs indicate address regions which will run at 1.19 MHz. (The 7M clock is divided by 6 instead of 3.)

4. The PAR23 output is the Maria register chip select signal.

3.3 DMA Operation

There are three major parts to DMA operation: Display List access, Display List List access, and Graphics/Map Data access. The levels of indirection in Maria DMA go as follows:

1. Microprocessor writes to Displaylist Pointer Pointer register (DPPH/L), which points to

2. Display List List, containing offset (zone size) and mode information, as well as a new DP which points to

3. Display List, containing a variable number of headers, each of which has width, palette, and position information, as well as a PP (Pixel Pointer), which points to either of two things:

    1. Graphics data which is loaded into the linerae, or

    2. Character map data, which fores the low byte of the address of one or two bytes of graphics data, depending on the state of the CWIDTH bit in the control register.

Display List (List) DMA begins when the control register is written to set it in the Run mode (rather than Inactive or either of the two test modes), after the DPP registers have been initialized. It is safest to do this during VBLANK, so that the first DMA action to take place will be the Display List List fetch. If DMA is turned on during on-screen time, the next End-Of-Scanline will start a Display List fetch, using previous register values.

The offset (zone size) value from the display list list header is added to the high byte of each effective graphics address to provide vertical offsetting of graphics. Each successive scanline of an object's graphics will be stored on a different 256-byte page of memory.

Merle II List ordering

Display List List format:

```
dpp:   <dli> <a12en> <e11en> < 0 > < Offset-- 4 bits >
                < dpl >
                < dph >
                   .
                   .
                   . (headers repeated: enough to fill screen)
```

Offset value (4 bits) represents (n+1) scanlines to be displayed. Put in a 15. to get 16. scenlines. Offset register value will decreeent each scenline. <e12en> and <a11en> control holy dma. If an effective grephics address has a12 or a11 set when their corresponding <a1xen> is set, zero grephics deta will be used end graphics fetching will be aborted. If <dli> is set, the NMI-pin will be esserted for one cpu cycle, one cycle after HALT- is released.

Display List format:

short format:

```
                < ppl >
                <  w  >          width field is non-zero
                < pph >
                < hpos>
                   .
                   .
                   . (Headers repeat until End Block)
```

```
w  = < P P P > < W W W W W >
```

width field may not be all zeroes

long foreet:

```
                < ppl >
                <  wl >
                < pph >
                <  w  >
                < hpos>
                   .
                   .
                   .
```

```
wl =  < we > < 1 > <ind> < 0 0 0 0 0 >
wm =  new value of wmode bit froe now on
ind = indirect mode for current header ONLY
w  =  < P P P > < W W W W W >
```

width field is not checked for all zeroes on 5-byte heeders.

end block:

```
                < ppl >
                <  0  >
```

Display lists end list lists must be in fest (RAM) eeeory.
Cherecter maps eust be in fest memory.

Graphics may be in slow (ROM) memory.
PPP represents 'Palette' code used throughout object graphics.
WWWWW represents negative of width; 11111 is one-byte wide.

3.3 DMA Operation (continued)

In direct (not Indirect) mode, the address (PPL and PPH) in the list element points to the actual graphic data to be stored into the line ram. The palette code will be stored along with each pixel which is not transparent. Width represents the number of bytes wide the object is.

The graphics data read will be interpreted in one of two ways, depending on the value of the WM (write-mode) flag. When WM = 0, each byte specifies four pixel cells of the linearm, when WM=1, each byte specifies two cells within the linerem. The final output video as read from the linerom will be interpreted according to the two RM (read-mode) bits in the control register. The following table lists the possible combinations of control bits, and how the linearm outputs finally map into address bits for the color ram.

MODE	WM	RM1	RM0	CRA4	CRA3	CRA2	CRA1	CRA0
160(A)	0	0	X	P2	P1	P0	D7	D6
							D5	D4
							D3	D2
							D1	D0
160B	1	0	X	P2	P3	P2	D7	D6
					D1	D0	D5	D4

MODE	WM	RM1	RM0	CRA4	CRA3	CRA2	CRA1	CRA0
320A	0	1	1	P2	P1	P0	D7	0
							06	0
							D5	0
							D4	0
							D3	0
							D2	0
							D1	0
							D0	0
320B	1	1	0	P2	0	0	07	03
							D6	02
							D5	01
							04	D0
320C	1	1	1	P2	D3	D2	07	0
							06	0
					D1	D0	D5	0
							D4	0
320D	0	1	0	P2	0	0	D7	P1
							06	P0
							D5	P1
							04	P0
							03	P1
							D2	P0
							D1	P1
							D0	P0

Pn represents the palette bits.
Dn represents the graphics data bits.
The topmost data in the table comes out first (is left-most on the screen).

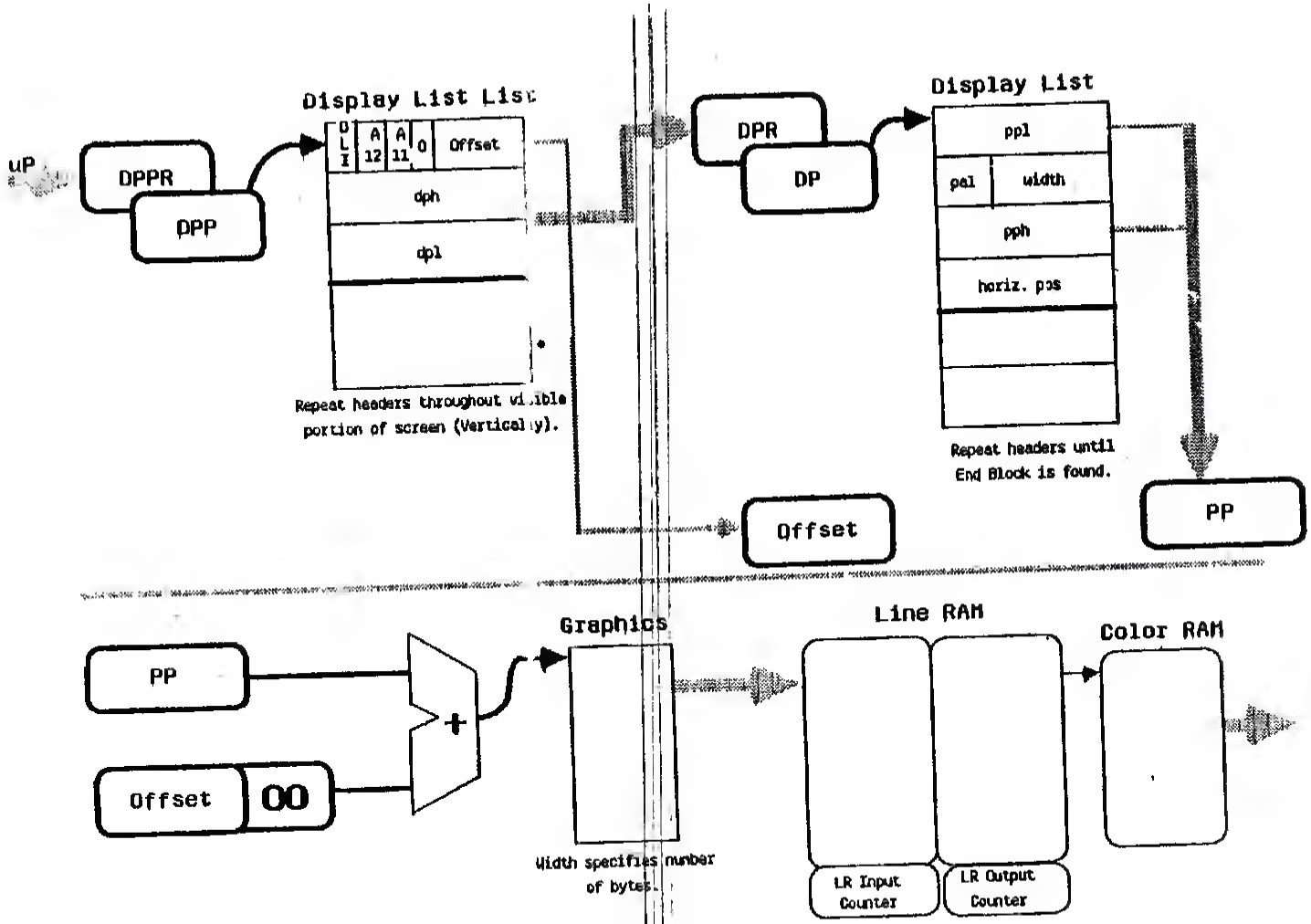
DMA Cycle Timing

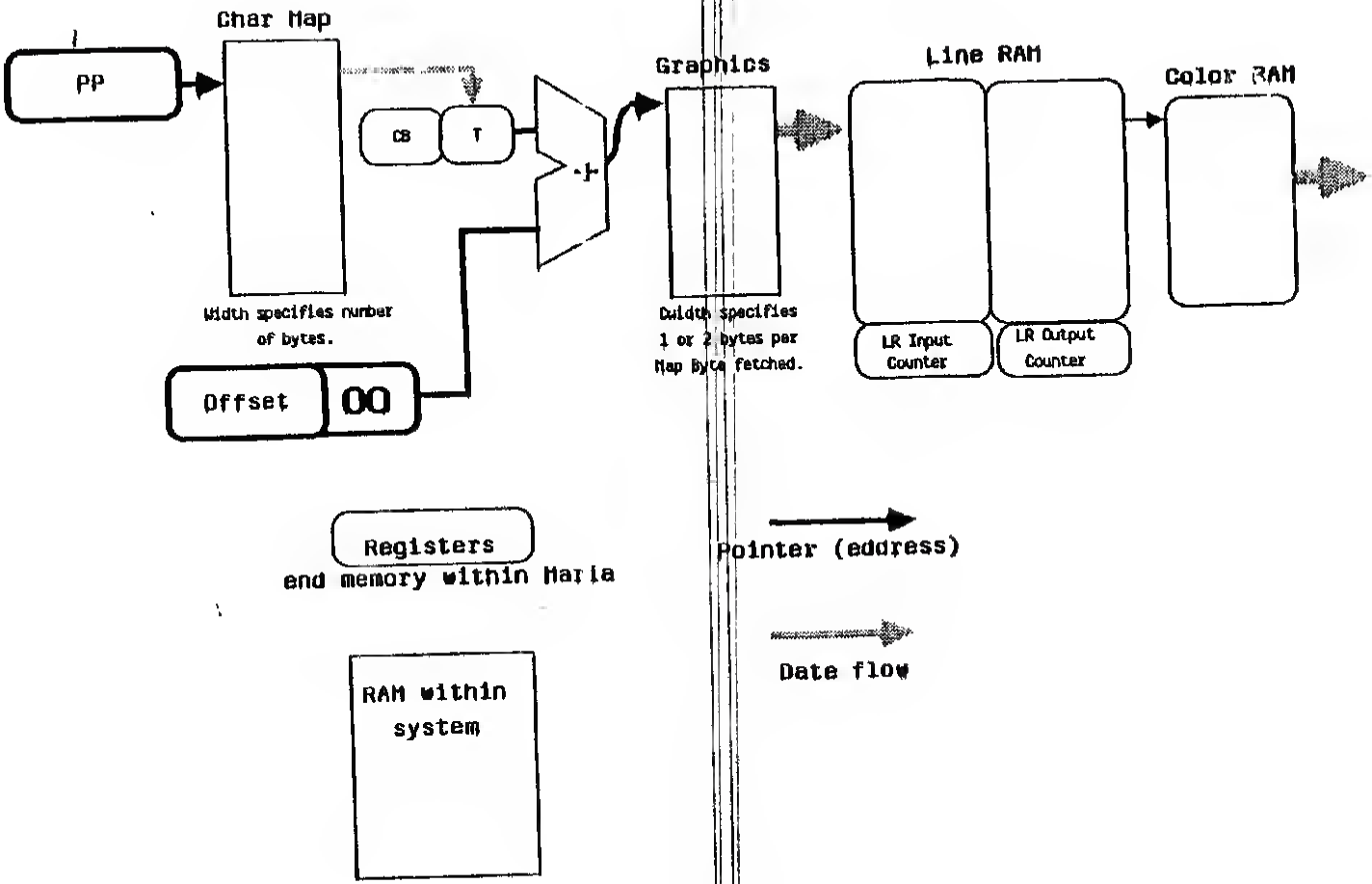
Short Header	8 cycles
Long Header	10 cycles
Graphics, per byte	3 cycles
Indirect map fetch	3 cycles (plus one or two graphics fetches)
DMA Startup	5-12 cycles
DMA Shutdown, short	13-17 cycles
DMA Shutdown, long	19-23 cycles (list-list fetch)
End-Of-VBlank DMA	7+ cycles

DMA/Sync Timing

End-Of-VBlank DMA is initiated on the trailing edge of VBlank.
Regular DMA is initiated on the leading edge of HBlank.
DMA will be aborted (to shutdown) on the leading edge of Border.
(See screen definition for counter values associated with these times.)

When the I bit is set in byte one of a list element, the address refers to a character map, instead of the graphic data itself. The value found at each succesive location in the map is concatenated with the contents of the CharBase register to form the address of a single byte (4 pixels) of character data to be read and stored in the line ram. The Width field specifies how many bytes are present in the map before continuing on to the next list element. If the CWIDTH bit in the control register is set, two consecutive graphics bytes are fetched for each character map byte.


Display List List
uP
DPPR
DPP
DLI
A12
A11
0
Offset
dph
dpl
Repeat headers throughout visible portion of screen (Vertically).
DPR
DP
Display List
ppl
pal
width
pph
horiz. pos
Repeat headers until End Block is found.
PP
Offset
Graphics
PP
Offset
00
Width specifies number of bytes.
Line RAM
LR Input Counter
LR Output Counter
Color RAM


Char Map
PP
CB
T
Graphics
Line RAM
Color RAM
Width specifies number of bytes.
Offset
00
Width specifies 1 or 2 bytes per Map byte fetched.
LR Input Counter
LR Output Counter
Registers and memory within Maria
Pointer (address)
Date flow
RAM within system

3.4 Line RAM Operation

Scan lines of video data are double-buffered in the line rams, with one being loaded while the other plays back. In order to make best use of this scheme, dma circuitry loads the "recording" buffer at high speeds according to directions found in a display list. Line RAM operation is as follows:

* The horizontal position is specified by the pixel address to which the graphic data is written into the line ram.

* While writing data to the line ram (with the KM bit of the control register zero) if any given pixel's color code is 00, that pixel's graphics and palette data are not written into the line ram. This transparency code allows objects to overlap and contain windows. The KM bit is set to 1 to defeat this transparency, for certain 320-wide modes.

* Prioritization of overlapping objects is achieved solely by the order in which the data is written to the line ram. The last object written will be on top.

* Horizontal resolution may be 160 by 2 bits per pixel, 160 by 4 bits per pixel (with the caveat that only 13 colors may be addressed by this scheme; XX00 always accesses the background color), 320 by 1 (intended for text), or 320 by 2.

* Automatic burst-clear sets all cells of the most recently displayed line ram buffer to zero after each scan line so that the programmer will not have to erase the old line image before entering a new one.

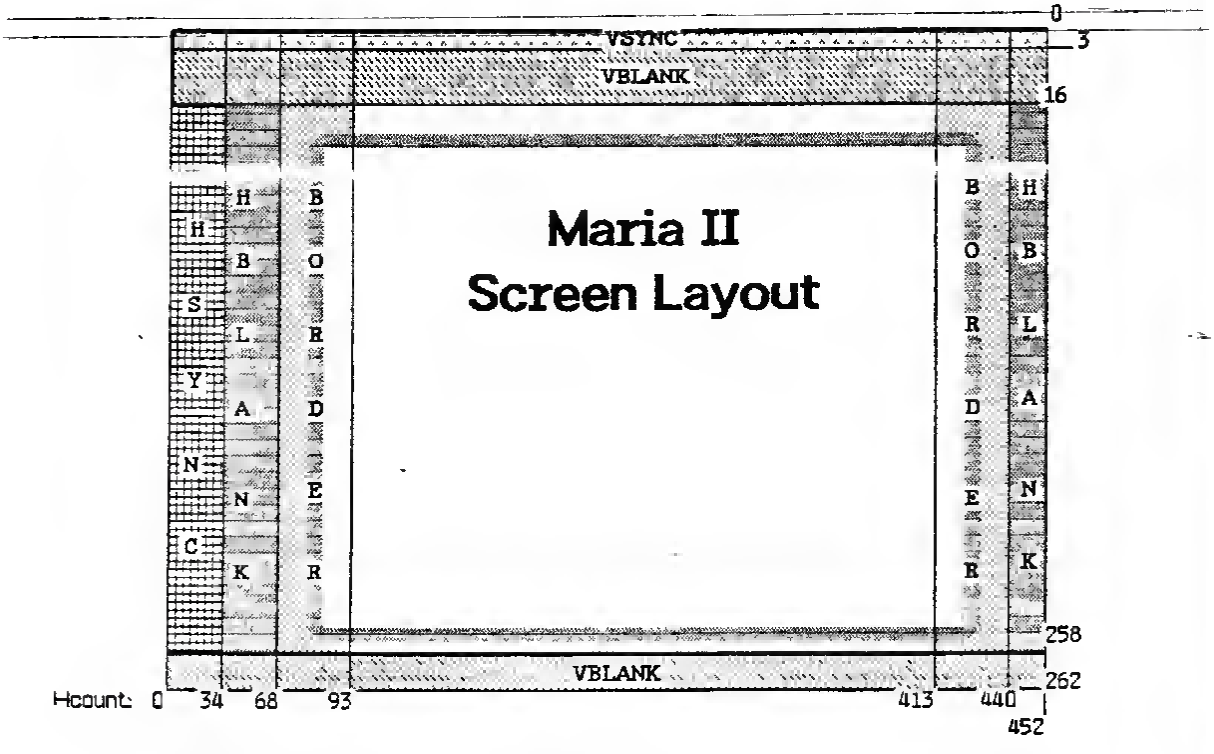
* Palette codes: Each pixel position, in addition to the 1 to 2 bits of graphic data, contains a 3-bit palette code, specifying one of eight palettes of 3 colors. The only conceptual difference between palette information and the 2 bits of graphic data is the speed with which it can change; a single palette is specified for the entire width of an object, while the graphic data may change on a pixel-by-pixel basis.

3.5 Color Map RAM

The output of the line RAM is finally interpreted into a five-bit address into a color mapping RAM organized as 25 x 8 bits. This RAM can be accessed at a 7 MHz rate (for 320-mode output) and can be written to almost transparently during on-screen time. This means that if the processor seizes the color RAM address selector to write in a new value, the previous output of the RAM will be held until the processor is done. This has the effect of stretching a legitimate pixel color on the screen horizontally for that one cycle, rather than have a wholly unexpected color (the one being written in) appear on the screen as a glitch.

The color RAM decoder is arranged such that any access to an address of XXX00 will select the same 'background' register in the RAM, hence the 25 byte addressing out of 5 bits, rather than 32 bytes.

The color RAM output is interpreted as four bits of luminance and four bits of chrominance. The least significant four bits are lum, while the upper four bits are color in a mapping arrangement similar to the TIA.



3.6 Video Output

The video output of the Maria chip is intended to be a very close approximation to the NTSC television standard video. The luminance portion of the signal is generated by a four-bit external resistor-ladder DAC. The chroma sub-carrier is a 3.58 MHz clock which is controllably phase-delayed to any of 15 angles with respect to the color burst signal which is output after each horizontal sync pulse. Also available are the options to turn off the sub-carrier for black and white video, and to turn off the sub-carrier for a black and white image. The SYNC and BLANK output pins are also available for summing to make the video signal. The SYNC signal is the logical exclusive-or of VSYNC and HSYNC.

4.0 Sentry Test Program

4.1 1702B chips shall he 100% tested to and perform digitally in accordance with the Sentry test vectors contained in Attachment A of this specification.
Production test sequences may be optimized hy the supplier provided that digital and parametric correlation to this referenced attachment is maintained and all changes are approved by the responsible Atari ASG director.

4.2 The order of Precedence shall he: 1) This specification sections 1, 2, 3, and 5; 2) Test vectors attached in Attachment A.

5.1 Input/Output D.C. Specifications -- 1702B

Parameter (Level)	Sym	Min	Max	Units	Conditions
Input Voltage - Low	Vil	---	0.8	Volts	except RWF, pin 39
Input Voltage - Low	Vil	-1.2	0.0	Volts	RWF, pin 39 only
Input Voltage - High	Vih	2.0	---	Volts	except MEN, pin 5
Input Voltage - High	Vih	2.7	---	Volts	MEN, pin 5 only
Output voltage - Low	Vol	---	0.4	Volts	
Output Voltage - High	Voh	2.4	---	Volts	
Output Current - Low	Iol	---	-2.0	mA	
Output Current - High	Ioh	---	+100	uA	
Output Leakage - TS	Its	---	+/-20	uA	
Power Supply Current	Icc	---	200	mA	25° C, Vdd=5.25v

5.2 Input/Output Timing Specifications:

Refer to figure 1702B Timing for these numbers:

Parameter (Time)	Sym	Min	Max	Units	Conditions
DMA Timing; Display List, Display ListList, Char Map: **					
ABout from ph2			80	nsec	C = 150pF
CS out from ph2			100	nsec	C = 25 pF
Din Req'd before ph2		15		nsec	
Din hold time		0		nsec	
Access time (CS)			165	nsec	
DMA timing; Graphic accesses:					
ABout from ph2			100	nsec	
CS out from ph2			120		

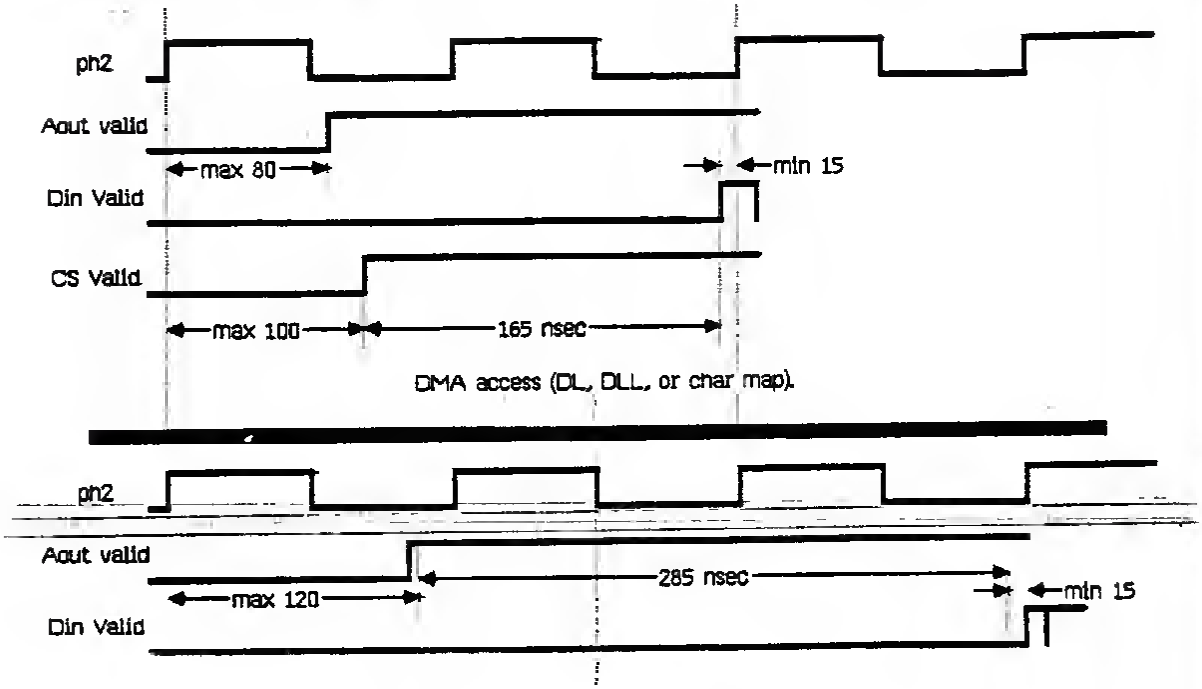
**Note: DMA Timing internal to 1702B. Above timing shown for reference only. See Page 31 of this specification.

uP Interface timing:					
AdrIn, r/w req'd before pck0		40		nsec	
CS out valid after pck0			40	nsec	
Din req'd before pck0 falls		40		nsec	
Dhold		0		nsec	
Dout valid before pck0 falls (Dout held through pclk2)		70		nsec	
Clock stretch timing:					
Adrs valid before pck0		60		nsec	
ABout rise/fall	Tarf	6	---	nsec	C = 150 pF
DBout rise/fall	Tdrf	---	25	nsec	C = 150 pF
PCLK0 rise/fall	Tprf	---	30	nsec	C = 25 pF
TIACLK rise/fall	Tprf	---	30	nsec	C = 25 pF
BLANK rise/fall	Tprf	---	30	nsec	C = 25 pF
LUMnF rise/fall	Tprf	---	30	nsec	C = 25 pF
SYNC rise/fall	Tprf	---	30	nsec	C = 25 pF
READY rise/fall	Tprf	---	30	nsec	C = 25 pF
HALTF rise/fall	Tprf	---	30	nsec	C = 25 pF
COLF rise/fall	Tprf	---	30	nsec	C = 25 pF

1702B timing

ph2 refers to internal Maria signal

pclk0 refers to 6502 phase 0 from Maria.



Graphics Access (ROM or RAM)

System Timing Requirements:

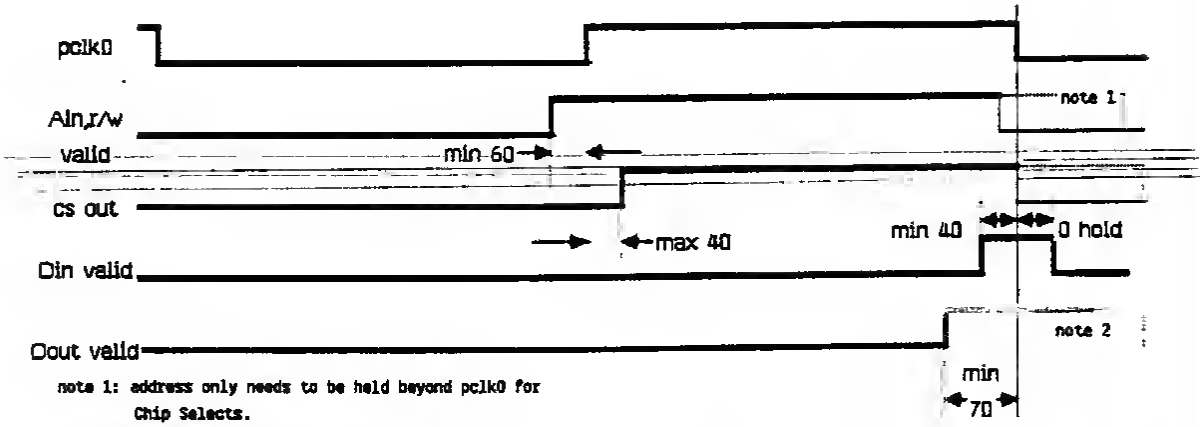
1. CLKIN (4 x 3.58 MHz): 70 nSEC PERIOD

2. DEL VOLTAGE OFFSET:

RANGE : 0 - 5.0 V

RESOLUTION: +/-2 nS

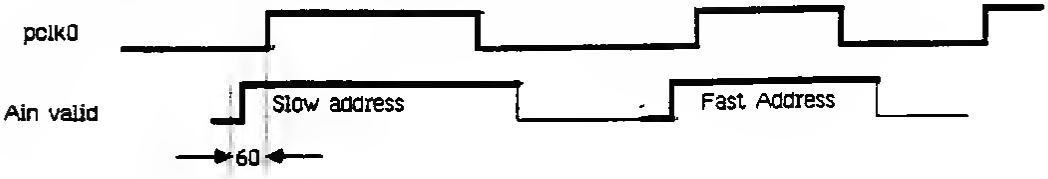
Microprocessor Interface Timing



note 1: address only needs to be held beyond pclk0 for Chip Selects.

Note2: Data out held through PCLK2.

Clock stretch timing for TIA and 6532 access: 7m divider shifts to by-6 from by-4 for pclk2 and following pclk1 time. In TIA mode divider stays in by-6 mode.



6.0 Absolute specifications:	Min	Max	Unit	
Voltage (any pin, referenced to VSS)	-0.5	+7.0	Volts	**
Static Test (any pin, 883 circuit)	500		Volts	
Storage Temperature (Ambient)	-25	+125	Deg C	
Operating Temperature (Ambient)	0	70	Deg C	
Operating Voltage (VDD)	4.75	5.25	Volts	

** Note: Voltage (pin 39, RWF only, referenced to VSS)	-1.2	+7.0	Volts	

Timing specifications (page 27) and timing diagrams (page 28) use ph2 edges as a reference point for DMA timing. This signal is internal to the "Maria" device and cannot be accessed externally. Pclock0 can be accessed externally and is similar to ph2 except that its edges are delayed from those of ph2.

The Sentry test program utilizes pclock0 as a reference point for DMA testing.

COLOR DELAY CIRCUIT

The color delay circuit provides a 3.58 MHz (oscillator input divided by 4) output with variable phase delay with respect to the Color Burst output, a zero-delay reference burst on the color pin during horizontal blank. When programmed for maximum delay (chroma field of color ram output = 15), the output on the color pin shall be adjustable to a phase delay time of 260 nsec by varying the DEL input pin between 0.5 and 6.0 volts. When programmed for a chroma value of between 1 and 14, the color output shall be delayed by incremental step values. When programmed for a chroma value of 0 (zero), the color pin output shall be DC.